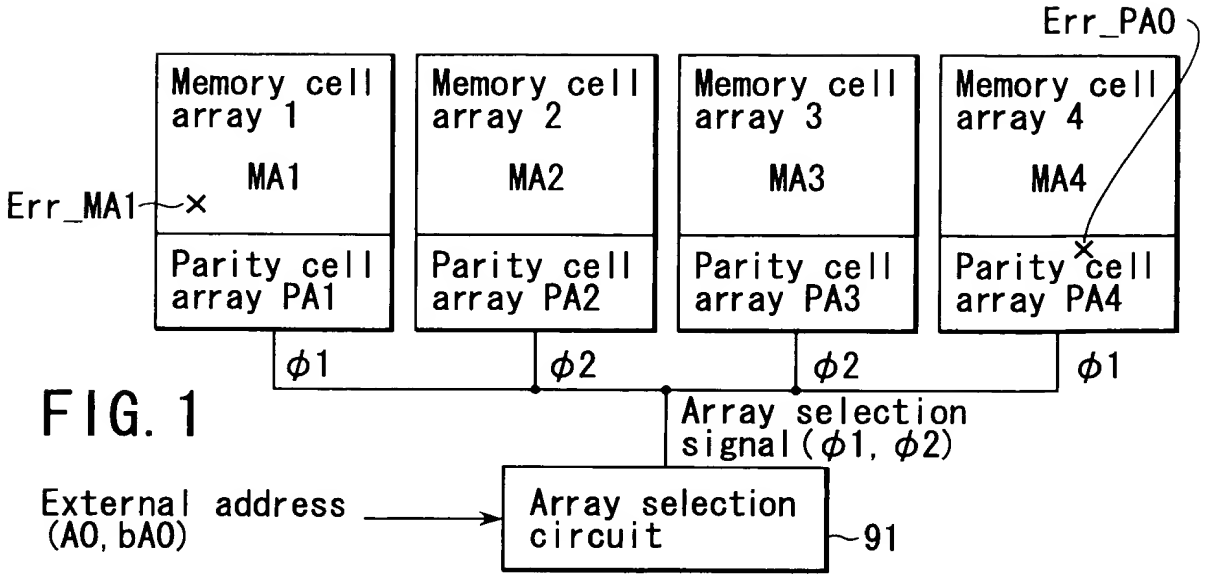


FIG. 1

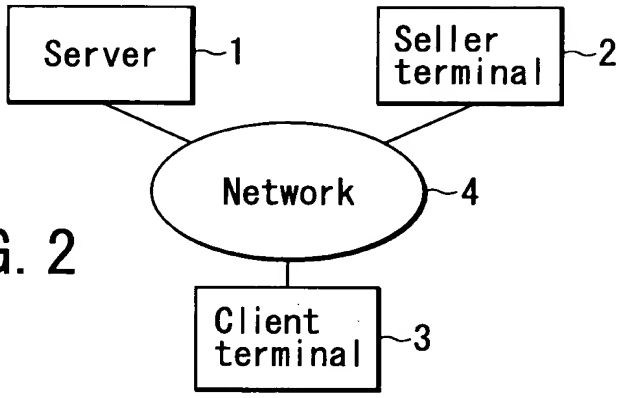


FIG. 2

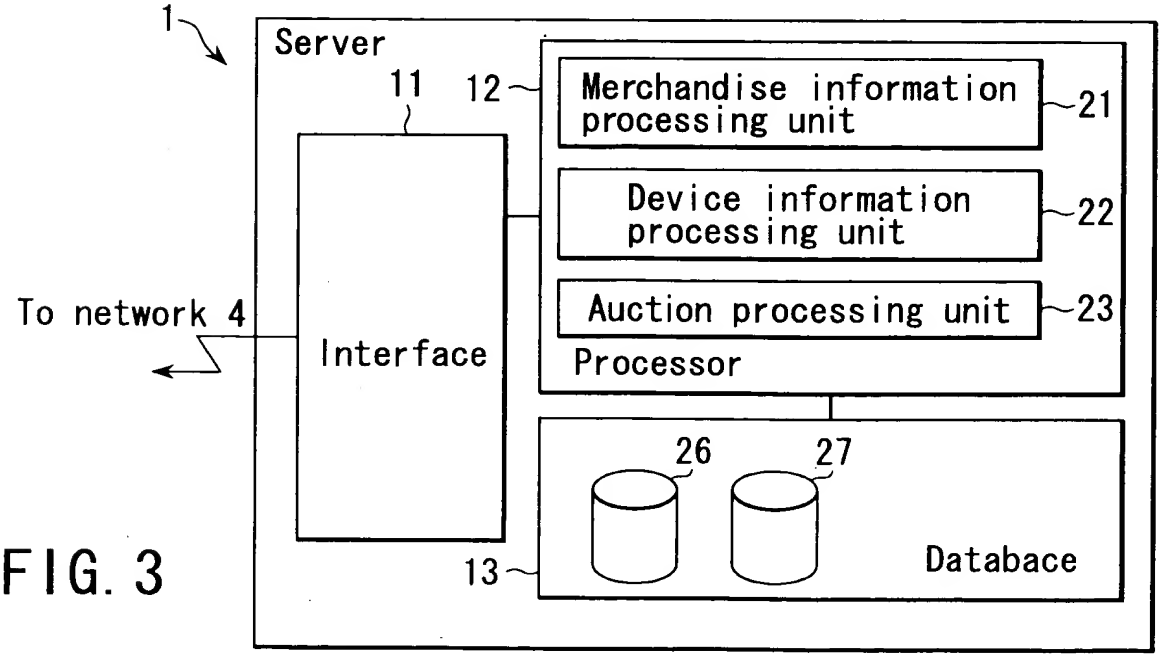


FIG. 3

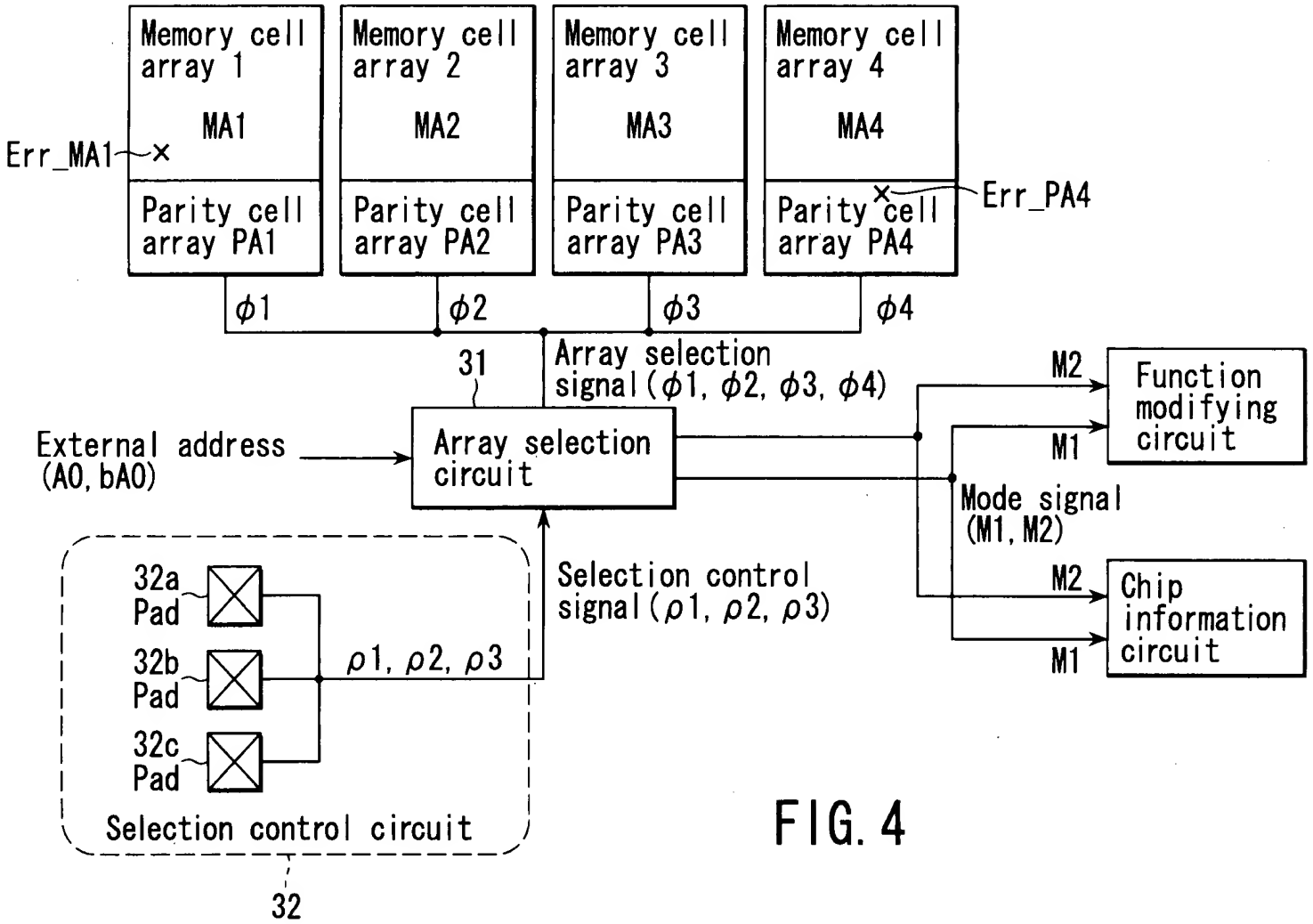

Memory cell array 1
MA1
Memory cell array 2
MA2
Memory cell array 3
MA3
Memory cell array 4
MA4
Err_MA1
Parity cell array PA1
Parity cell array PA2
Parity cell array PA3
Parity cell array PA4
Err_PA4
φ1
φ2
φ3
φ4
31
Array selection signal (φ1, φ2, φ3, φ4)
External address (A0, bA0)
Array selection circuit
M2
M1
Function modifying circuit
Mode signal (M1, M2)
M2
M1
Chip information circuit
Selection control signal (ρ1, ρ2, ρ3)
32a Pad
32b Pad
32c Pad
ρ1, ρ2, ρ3
Selection control circuit
32

FIG. 4

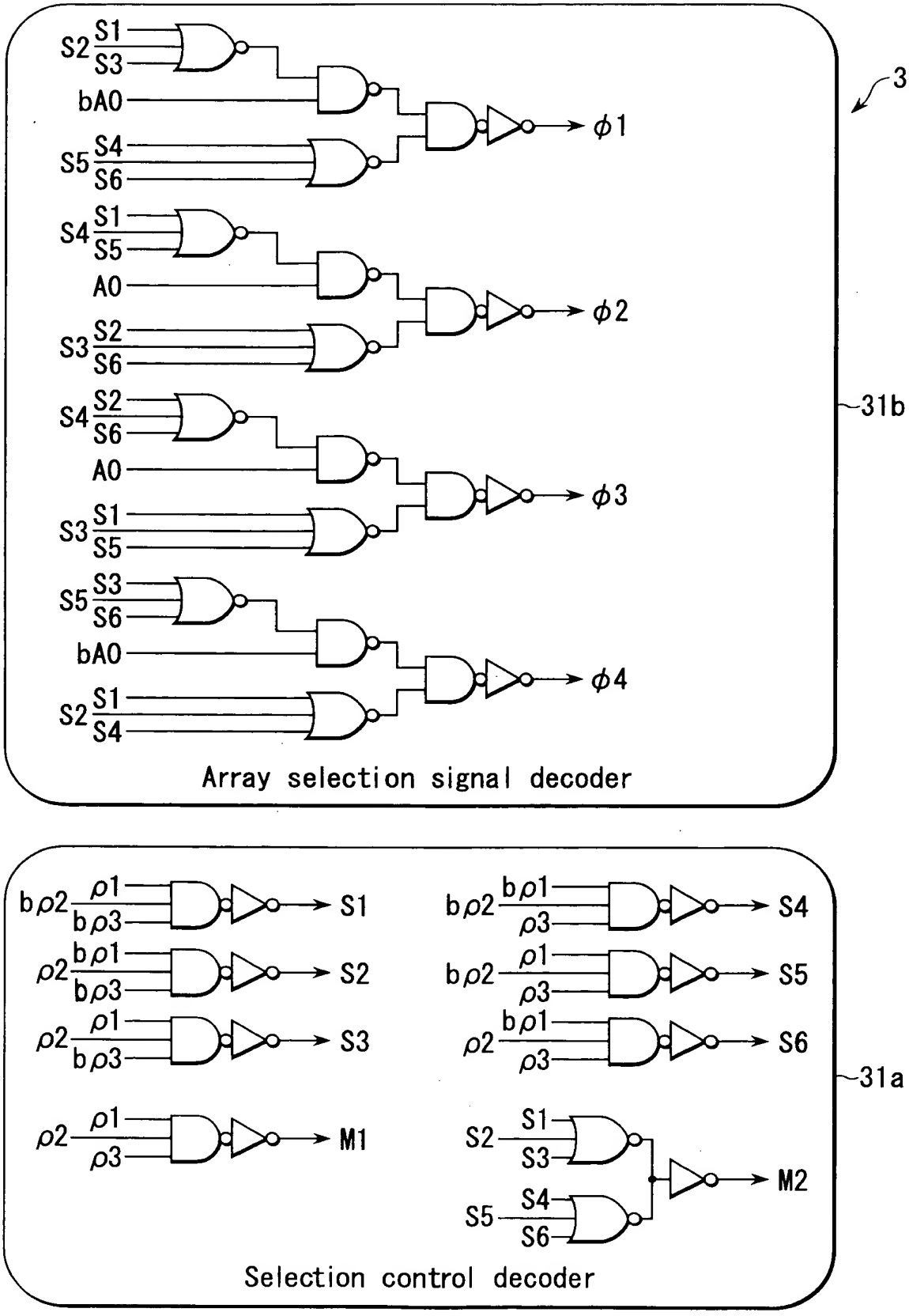

S2
S1
S3
bA0
S5
S4
S6
φ1
S4
S1
S5
A0
S3
S2
S6
φ2
S4
S2
S6
A0
S3
S1
S5
φ3
S5
S3
S6
bA0
S2
S1
S4
φ4
Array selection signal decoder
31
31b
bρ2
ρ1
bρ3
S1
ρ2
bρ1
bρ3
S2
ρ2
ρ1
bρ3
S3
ρ2
ρ1
ρ3
M1
bρ2
bρ1
ρ3
S4
bρ2
ρ1
ρ3
S5
ρ2
bρ1
ρ3
S6
S2
S1
S3
S5
S4
S6
M2
Selection control decoder
31a

FIG. 5

	Selected array	$\phi 1$	$\phi 2$	$\phi 3$	$\phi 4$	$\rho 1$	$\rho 2$	$\rho 3$	A0	M1	M2
1	MA1 & MA2	1	1	0	0	1	0	0	–	0	1
2	MA1 & MA3	1	0	1	0	0	1	0	–	0	1
3	MA1 & MA4	1	0	0	1	1	1	0	–	0	1
4	MA2 & MA3	0	1	1	0	0	0	1	–	0	1
5	MA2 & MA4	0	1	0	1	1	0	1	–	0	1
6	MA3 & MA4	0	0	1	1	0	1	1	–	0	1
7	MA1 & MA4	1	0	0	1	0	0	0	1	0	0
8	MA1 & MA2	1	0	0	1	1	1	1	1	1	1
9	MA2 & MA3	0	1	1	0	0	0	0	0	0	0
10	MA2 & MA3	0	1	1	0	1	1	1	0	1	1

Default:
A0 = "1"Array MA1 & MA4 are selected
A0 = "0"Array MA2 & MA3 are selected

FIG. 6

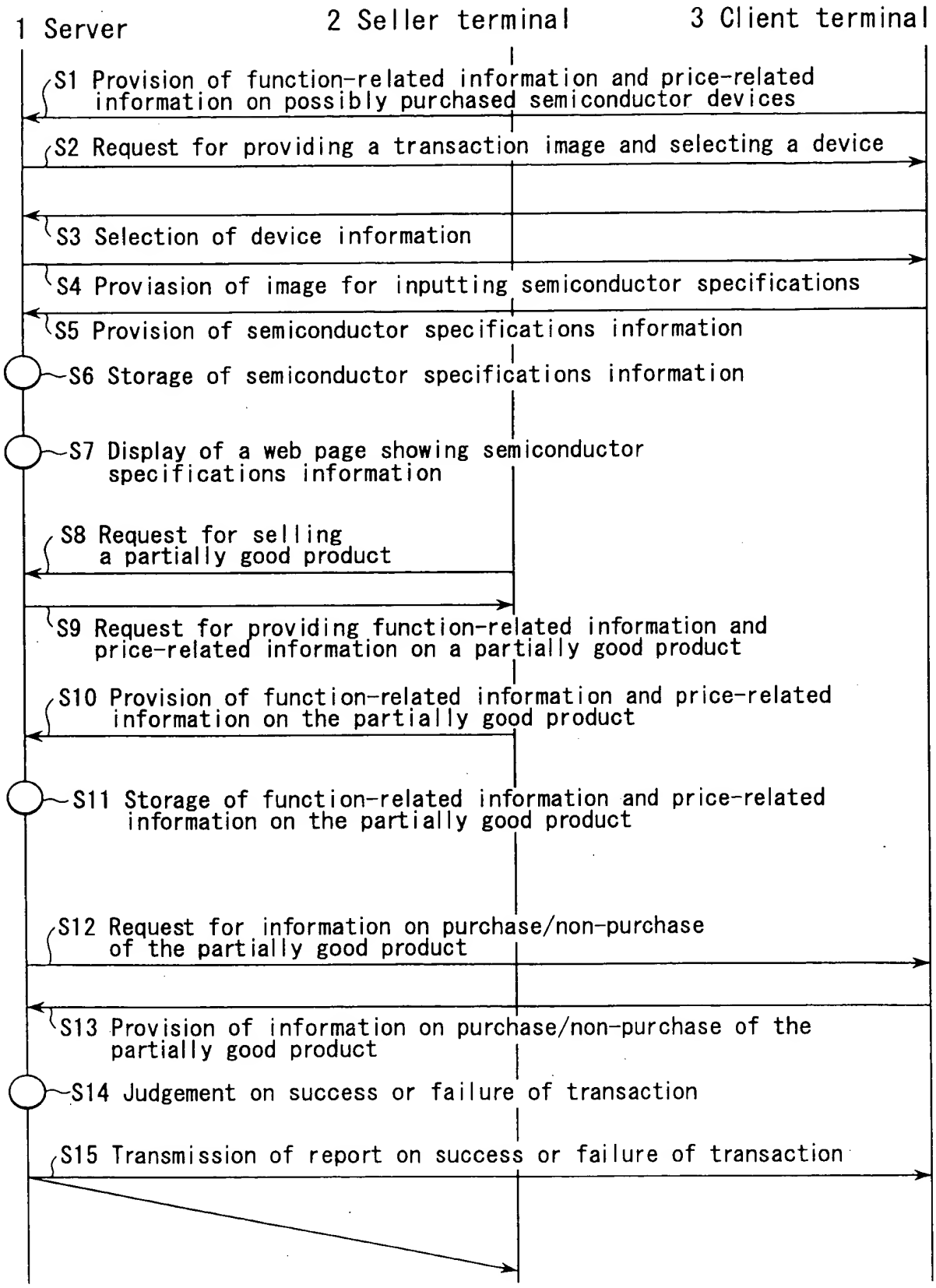

1 Server
2 Seller terminal
3 Client terminal
S1 Provision of function-related information and price-related information on possibly purchased semiconductor devices
S2 Request for providing a transaction image and selecting a device
S3 Selection of device information
S4 Proviasion of image for inputting semiconductor specifications
S5 Provision of semiconductor specifications information
S6 Storage of semiconductor specifications information
S7 Display of a web page showing semiconductor specifications information
S8 Request for selling a partially good product
S9 Request for providing function-related information and price-related information on a partially good product
S10 Provision of function-related information and price-related information on the partially good product
S11 Storage of function-related information and price-related information on the partially good product
S12 Request for information on purchase/non-purchase of the partially good product
S13 Provision of information on purchase/non-purchase of the partially good product
S14 Judgement on success or failure of transaction
S15 Transmission of report on success or failure of transaction

FIG. 7

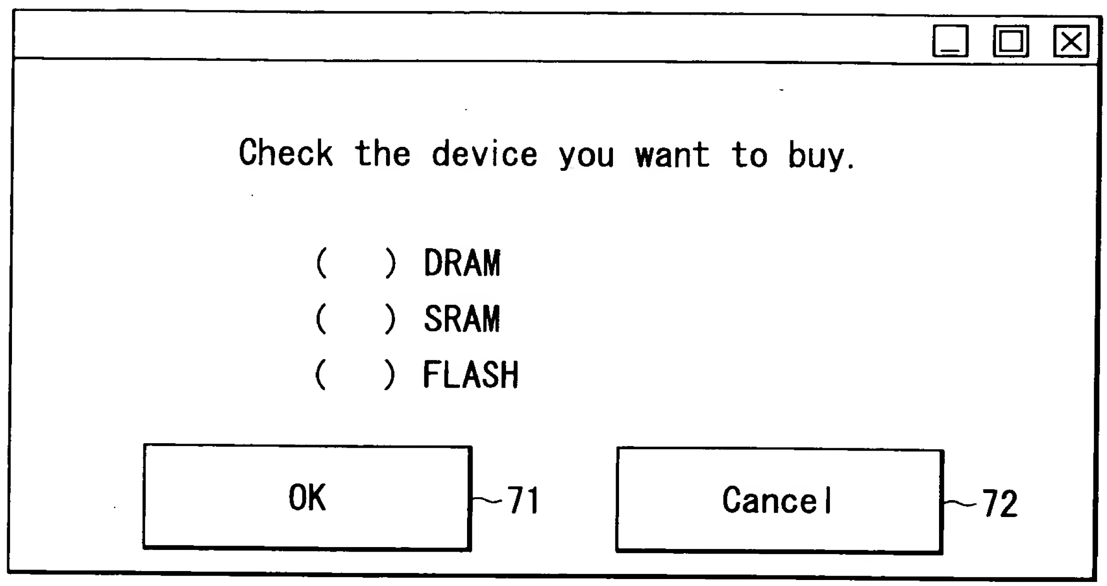

Check the device you want to buy.
( ) DRAM
( ) SRAM
( ) FLASH
OK
71
Cancel
72

FIG. 8

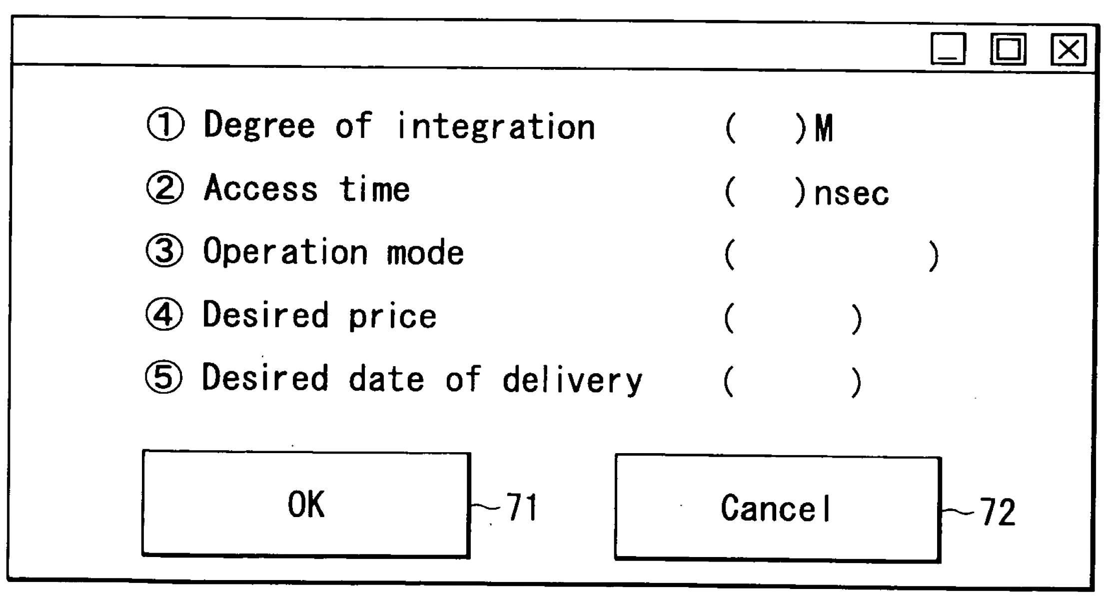
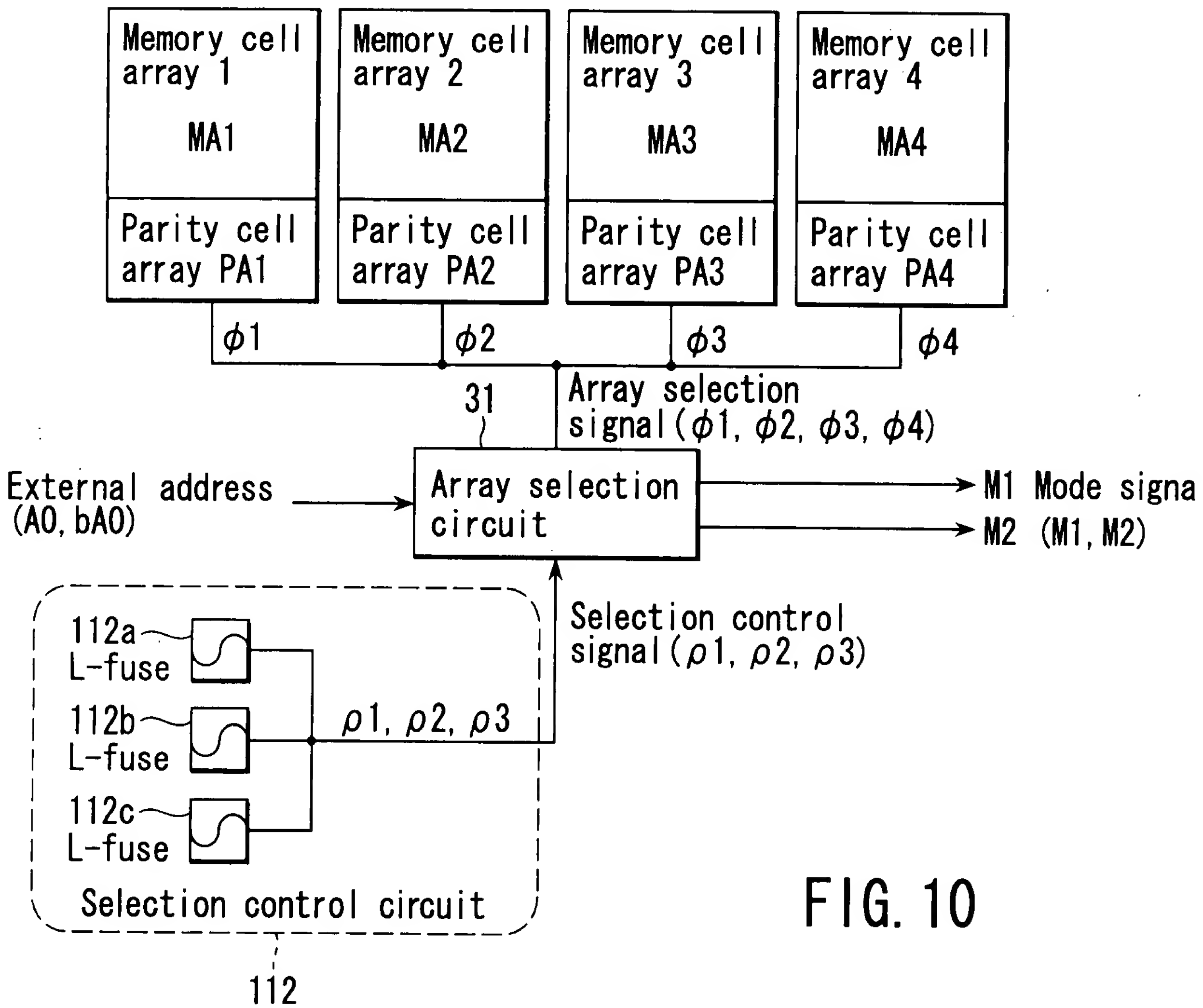

① Degree of integration ( )M
② Access time ( )nsec
③ Operation mode ( )
④ Desired price ( )
⑤ Desired date of delivery ( )
OK
71
Cancel
72

FIG. 9



Memory cell array 1
MA1
Parity cell array PA1
Memory cell array 2
MA2
Parity cell array PA2
Memory cell array 3
MA3
Parity cell array PA3
Memory cell array 4
MA4
Parity cell array PA4
φ1
φ2
φ3
φ4
31
Array selection signal (φ1, φ2, φ3, φ4)
External address (A0, bA0)
Array selection circuit
M1 Mode signal
M2 (M1, M2)
112a L-fuse
112b L-fuse
112c L-fuse
ρ1, ρ2, ρ3
Selection control signal (ρ1, ρ2, ρ3)
Selection control circuit
112

FIG. 10

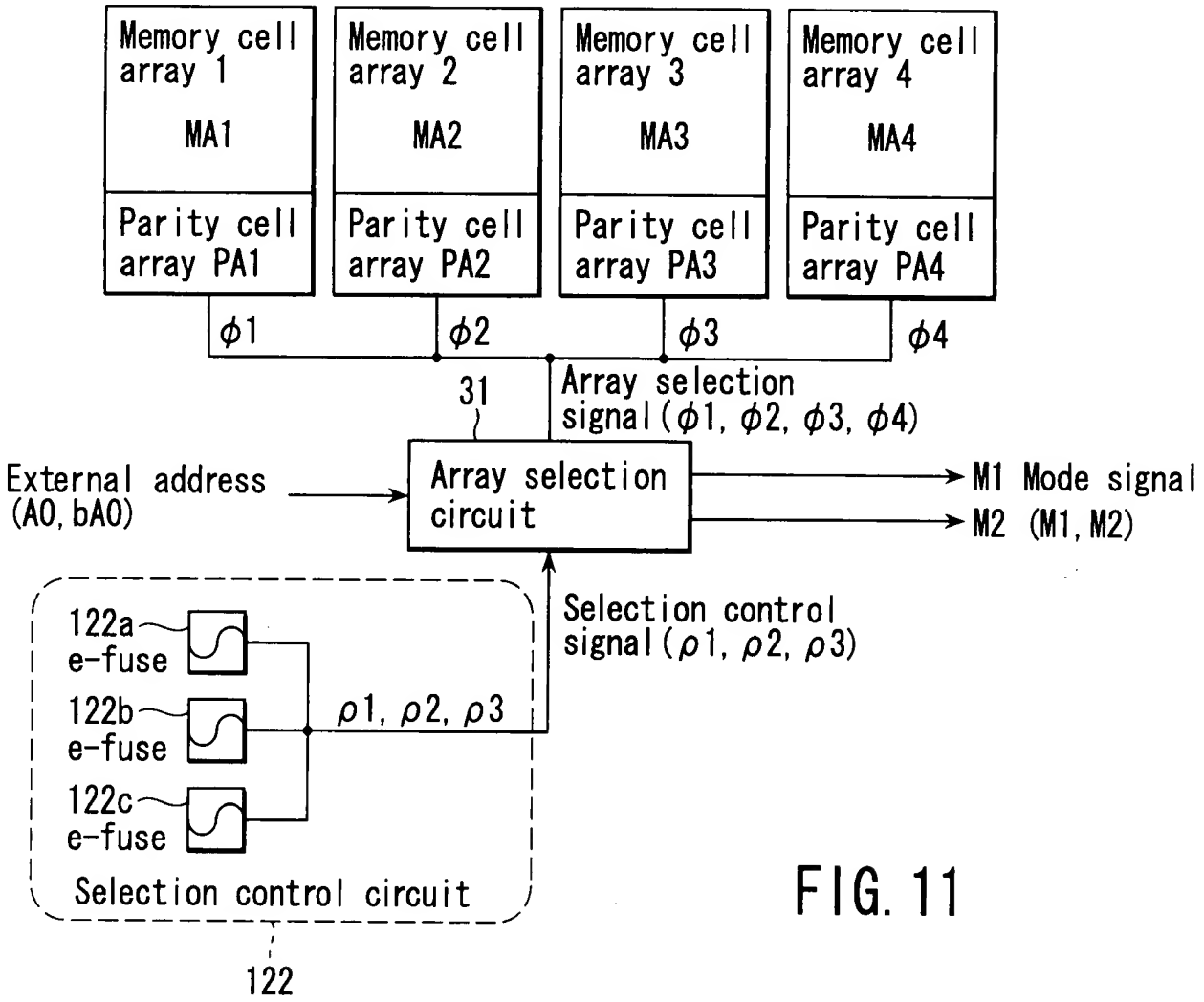

Memory cell array 1
MA1
Memory cell array 2
MA2
Memory cell array 3
MA3
Memory cell array 4
MA4
Parity cell array PA1
Parity cell array PA2
Parity cell array PA3
Parity cell array PA4
φ1
φ2
φ3
φ4
31
Array selection signal (φ1, φ2, φ3, φ4)
External address (A0, bA0)
Array selection circuit
M1 Mode signal
M2 (M1, M2)
Selection control signal (ρ1, ρ2, ρ3)
122a e-fuse
122b e-fuse
122c e-fuse
ρ1, ρ2, ρ3
Selection control circuit
122

FIG. 11

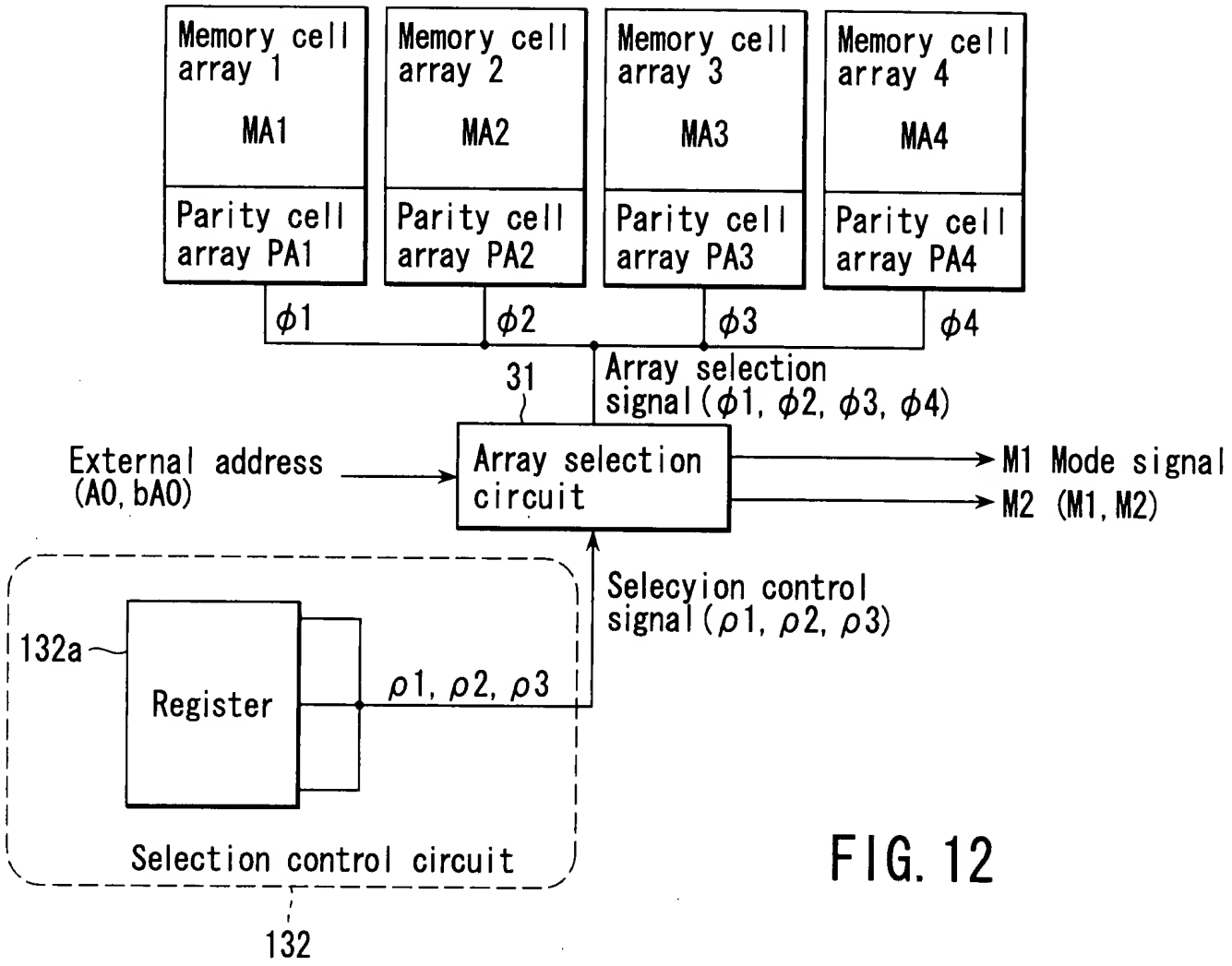

Memory cell array 1
MA1
Parity cell array PA1
Memory cell array 2
MA2
Parity cell array PA2
Memory cell array 3
MA3
Parity cell array PA3
Memory cell array 4
MA4
Parity cell array PA4
φ1
φ2
φ3
φ4
31
Array selection signal (φ1, φ2, φ3, φ4)
External address (A0, bA0)
Array selection circuit
M1 Mode signal
M2 (M1, M2)
Selecyion control signal (ρ1, ρ2, ρ3)
132a
Register
ρ1, ρ2, ρ3
Selection control circuit
132

FIG. 12

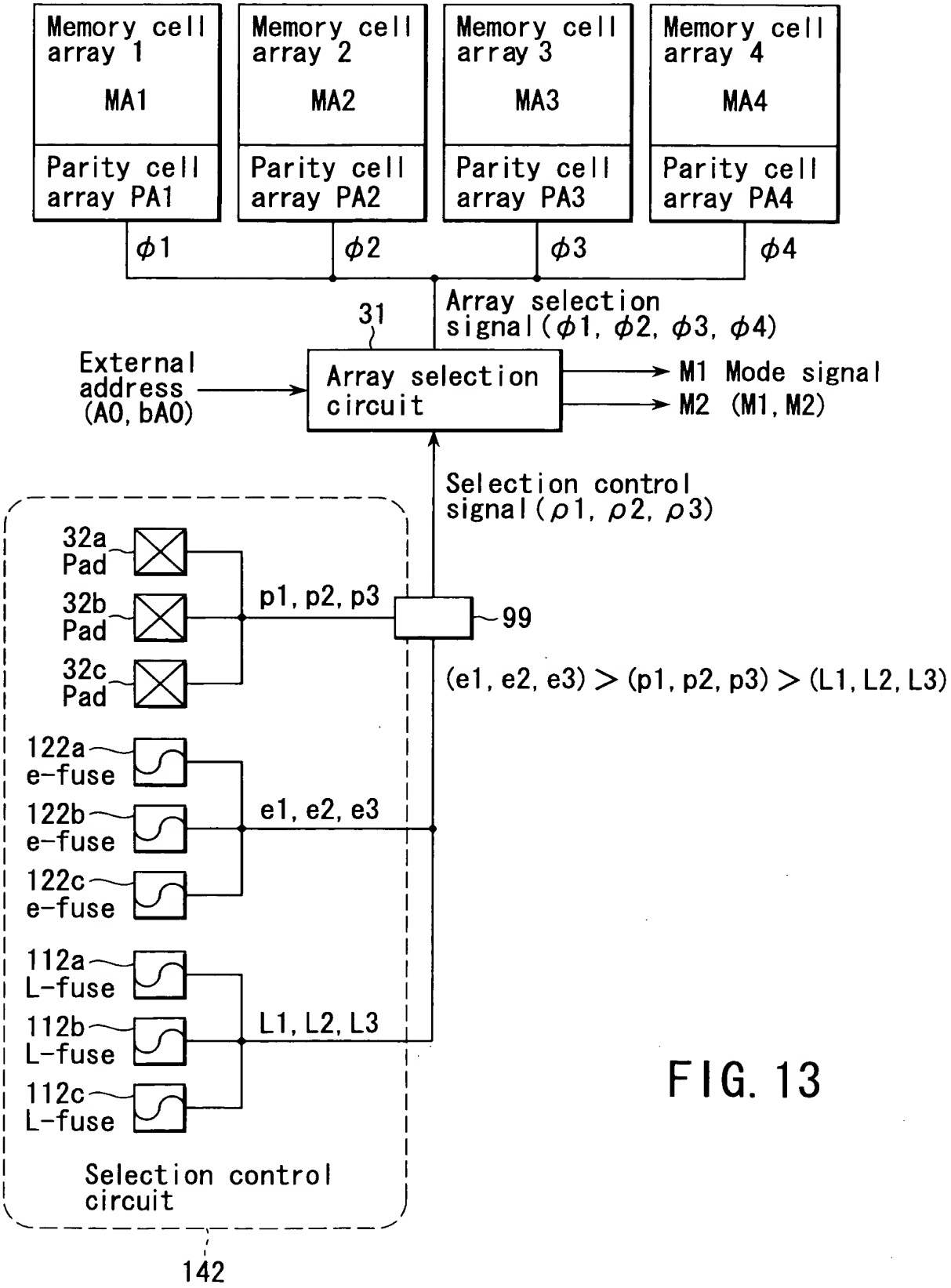

Memory cell array 1
MA1
Parity cell array PA1
Memory cell array 2
MA2
Parity cell array PA2
Memory cell array 3
MA3
Parity cell array PA3
Memory cell array 4
MA4
Parity cell array PA4
φ1
φ2
φ3
φ4
31
Array selection signal (φ1, φ2, φ3, φ4)
External address (A0, bA0)
Array selection circuit
M1 Mode signal
M2 (M1, M2)
Selection control signal (ρ1, ρ2, ρ3)
32a Pad
32b Pad
32c Pad
p1, p2, p3
99
(e1, e2, e3) > (p1, p2, p3) > (L1, L2, L3)
122a e-fuse
122b e-fuse
122c e-fuse
e1, e2, e3
112a L-fuse
112b L-fuse
112c L-fuse
L1, L2, L3
Selection control circuit
142

FIG. 13